

## REMARKS

Applicant's representatives present the claim amendments herein after final rejection.

Regarding Claim 11, the Examiner states that Smith teaches a method for sharing data between a first controller memory module and a second controller memory module, comprising providing a first shared path in a first channel interface module, wherein the shared path has a switchable component for determining which data is to be routed over the shared part. The following relate to the above recited components:

- (a) The first and second controller memory modules apparently are asserted by the Examiner to be all the components 215-280. Thus, the Examiner is apparently asserting that the first controller memory module is substantially the entire mobile computer 110, and the second controller memory module is the components: PCI-to-PCI bridge 260, secondary bus 262, PCI-to-ISA bridge 270, and slave DMA controller 280. However, Applicant's representatives are not clear as to which components the Examiner is asserting as the first controller memory module, and which components the Examiner is asserting as the second controller memory module.
- (b) The first shared path (in a first channel interface module) is identified in one portion of the Examiner's response as the primary PCI bus 240 and the secondary bus 262. However, an alternative interpretation of the Examiner's comments might be that the first shared path is the primary PCI bus 240, and the first channel interface module is the secondary PCI bus 262. Since this primary PCI bus 240 is not *in* the secondary bus 262, this alternative interpretation appears inappropriate. However, in another portion of the Examiner's response the first shared path is apparently identified as: the primary PCI bus 240, the secondary bus 262, the bridge 260.
- (c) The Examiner does not identify a component(s) of Smith corresponding to the "first channel interface module". However, since Claim 11 recites that the "first shared path" is *in* the first channel interface, the first channel interface must presumably at least include the components identified by one of the Examiner's interpretations of the "first shared path". However, it is unclear what Examiner intends the "first channel interface module" to correspond to in Smith.

- (d) The Examiner further identifies the "switchable component", apparently, as Smith's central DMA 215, and the Examiner cites column 8, lines 20-30 to substantiate his assertion that the DMA 215 can be the switchable component. For completeness, this Smith passage is recited here:

"Once the slave DMA controller 280 has transmitted the appropriate data to the central DMA controller 215, control passes to a sub-method block 340 wherein the central DMA controller 215, under the direction of the state machine 217, transfers the appropriate channel data, including the channel number, the base address and count data, and the data to be stored in the mode register, to the slave DMA controller 280. This channel data is transmitted to the slave DMA controller 280 via the primary PCI bus 240, the PCI-to-PCI bridge 260, the secondary PCI bus 262, and the PCI-to-ISA bridge 270."

Thus, since Smith's central DMA controller 215 is not part of the Examiner's identified "first shared path", the Examiner is presumably interpreting the word "has" in the Claim 11 phrase "the shared path *has* a switchable component for determining which data is to be routed over the shared path" as being equivalent to "associated therewith".

Applicant's representatives have attempted to address the Examiner's rejection of Claim 11 as follows. Claim 11 has been amended to recite that: (a) the first shared path **includes** the switchable component, and (b) the first shared path is included on a data path between the first and second controller memory modules. Accordingly, when (a) and (b) are taken together, it is believed that neither of the Smith DMAs 215, 280 can be interpreted as including the switchable component. Thus, it is believed that the Examiner's rejection of Claim 11 is overcome. However, in the event that the Examiner disagrees with the above reasoning, it is respectfully requested that the Examiner more clearly identify in Smith the features that are asserted as corresponding to components and limitations of Claim 11.

Regarding Claim 12, the Examiner states that Smith teaches providing a second shared path in a second channel interface module wherein the second shared path is (as best as can be understood) is identified as the DMA request line 298. However, it is believed that the Examiner did not identify the "second channel interface module". Accordingly, it is

respectfully requested that the Examiner explicitly identify the "second channel interface module". Additionally, the Examiner states that Smith teaches transferring "second data" between the first and second controller memory modules using each of the direct memory access engines, wherein the second data passes through the second shared path. However, the Examiner identifies the second shared path in this latter context as being "bus 216, DMA 212-213". It is assumed that "bus 216, DMA 212-213" was stated in error by the Examiner since Fig. 2 of Smith has no bus 216, no DMA 212, and no DMA 213. Additionally, there is no 212, 213 nor 216 disclosed in Smith's specification. Thus, it is assumed that the Examiner's (apparent) first identification of the "second shared path", as request line 298, is what is intended.

Applicant's representatives have attempted to address the Examiner's rejection of Claim 12 as follows. Claim 12 has been amended to recite that: (a) the second shared path is included on a data path between the first and second controller memory modules, and (b) the second shared path includes a second switchable component for determining which data is to be routed over the second shared path. Assuming the first and second controller memory modules are as the Examiner identified them in Claim 11 (or as best as can be determined), it is believed that the combination of the limitations (a) and (b) overcomes the Examiner's rejection of Claim 12. In particular, DMA request line 298 does not include a "second switchable component". Moreover, note that this limitation was recited in previously entered Claim 21.

Regarding Claim 13, the Examiner states that Smith teaches connecting the first and second channel interface modules and the first and second controller memory modules to a passive backplane. The Examiner's justification for this assertion is "see figure 2". However, it is respectfully submitted that figure 2 of Smith does not teach or suggest using a passive backplane as this term is used in the art. As described in the previous Amendment and Response provided to the Examiner, a passive backplane is described in the following definition of "backplane":

(bak'plān) (n.) A circuit board containing sockets into which other circuit boards can be plugged in. In the context of PCs, the term backplane refers to the large circuit board that contains sockets for expansion cards.

Backplanes are often described as being either *active* or *passive*. Active backplanes contain, in addition to the sockets, logical circuitry that performs computing functions. In contrast, passive backplanes contain almost no computing circuitry.

Traditionally, most PCs have used active backplanes. Indeed, the terms *motherboard* and *backplane* have been synonymous. Recently, though, there has been a move toward **passive backplanes**, with the active components such as the CPU inserted on an additional card. Passive backplanes make it easier to repair faulty components and to upgrade to new components.

<http://www.webopedia.com/TERM/B/backplane.html>

Another description of "passive backplane" is as follows:

All the active circuitry that [in] is normally found on an "active" PC motherboard (such as the CPU) is moved to a plug-in card. The new motherboard has nothing on it other than connectors, and is referred to as a **passive backplane**. The chance of a passive backplane failing is very low. Also referred to as "slot card" technology. (8/97)

<http://topcc.org/glossary/glossp.htm>

Applicant's representatives can, if the Examiner desires, supply numerous other similar descriptions of passive backplanes. As best as can be understood, presumably the Examiner is suggesting that Smith's docketing interface 255 is a passive backplane. However, it is believed that no where in Smith is there any teaching or suggestion of the docketing interface 255 being a passive backplane. In fact, the only description of the docketing interface 255 is as follows:

"The notebook computer 110 engages with the docking station 120 (also shown in FIG. 2 as enclosed within a dashed line) via a docking interface 255. The docking interface 255 preferably comprises an electrical connector which electrically connects the notebook computer 110 to the docking station 120. A PCI-to-PCI bridge 260 within the docking station 120 connects to the docking

interface 255 to provide an interface between the primary PCI bus 240 within the notebook computer 110 and a secondary PCI bus 262 within the docking station 120. The PCI-to-PCI bridge 260 preferably includes a repeater as well as other connector and conventional interface circuitry to provide for error free communication between the primary PCI bus 240 and the secondary PCI bus 262. The PCI-to-PCI bridge 260 is preferably constructed in accordance with the specifications laid out in revision 1.0 of the PCI-to-PCI bridge architecture specification available from PCI special interest group, N/SHS3-15A, 5200 N.E. Elam Young Parkway, Hillsboro, Oreg. 97124-6497." (Smith, col.5, ln. 57 through col. 6, ln. 8)

Accordingly, if the Examiner still persists in asserting that Smith's docketing interface 255 is a passive backplane, then it is respectfully requested that the Examiner provide substantiation for such an assumption.

Additionally, since the Examiner has not identified the "first channel interface module" in Smith, it is respectfully requested that if the Examiner persists in rejecting Claim 13, that the Examiner identify the "first channel interface module" in manner consistent with the limitations of Claim 13.

Regarding Claim 14, this claim has been amended to recite that:

- (a) Each of the first and second controller memory modules is for controlling communication of storage data between one or more host computers and one or more storage devices;
- (b) "The first channel interface module is directed by at least one of the first and second controller memory modules to communicate with a first of the host computers and a first of the data storage devices, so that the first channel interface module is operational for sending and receiving storage data between the first host computer and the first storage device"; and
- (c) "Direct communications" via a "communications interface" is permitted between the first and second controller memory modules wherein the "direct communications" are not routed through the first host computer.

It is believed that Claim 14 now overcomes the Examiner's rejections, and accordingly, Claim 14 is now in condition for allowance.

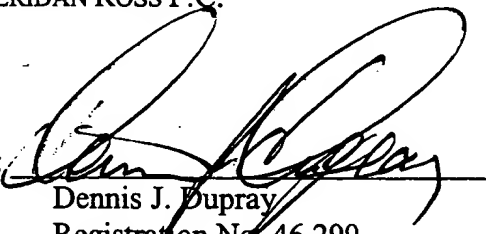
Since Claims 15 through 22 are dependent upon at least one of the allowable Claims 11 through 14, it is believed that Claims 15 through 22 are now also in condition for allowance.

Since all claims are now believed to be in condition for allowance, Applicant's representatives request reconsideration of the present application, and prompt allowance thereof. It is believed that no fees are due with this transmittal, but in the event that any fees are due, please charge Deposit Account No. 19-1970. Since this transmittal is timely filed within the allotted time for an Advisory Action, it is requested that the Examiner contact the undersigned as soon as possible regarding whether the Examiner will allow the present application, and/or for determining how best to put the present application in condition for allowance.

Respectfully submitted

SHERIDAN ROSS P.C.

By:



Dennis J. Dupray  
Registration No. 46,299  
1560 Broadway, Suite 1200  
Denver, Colorado 80202  
Phone: 303-863-9700

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